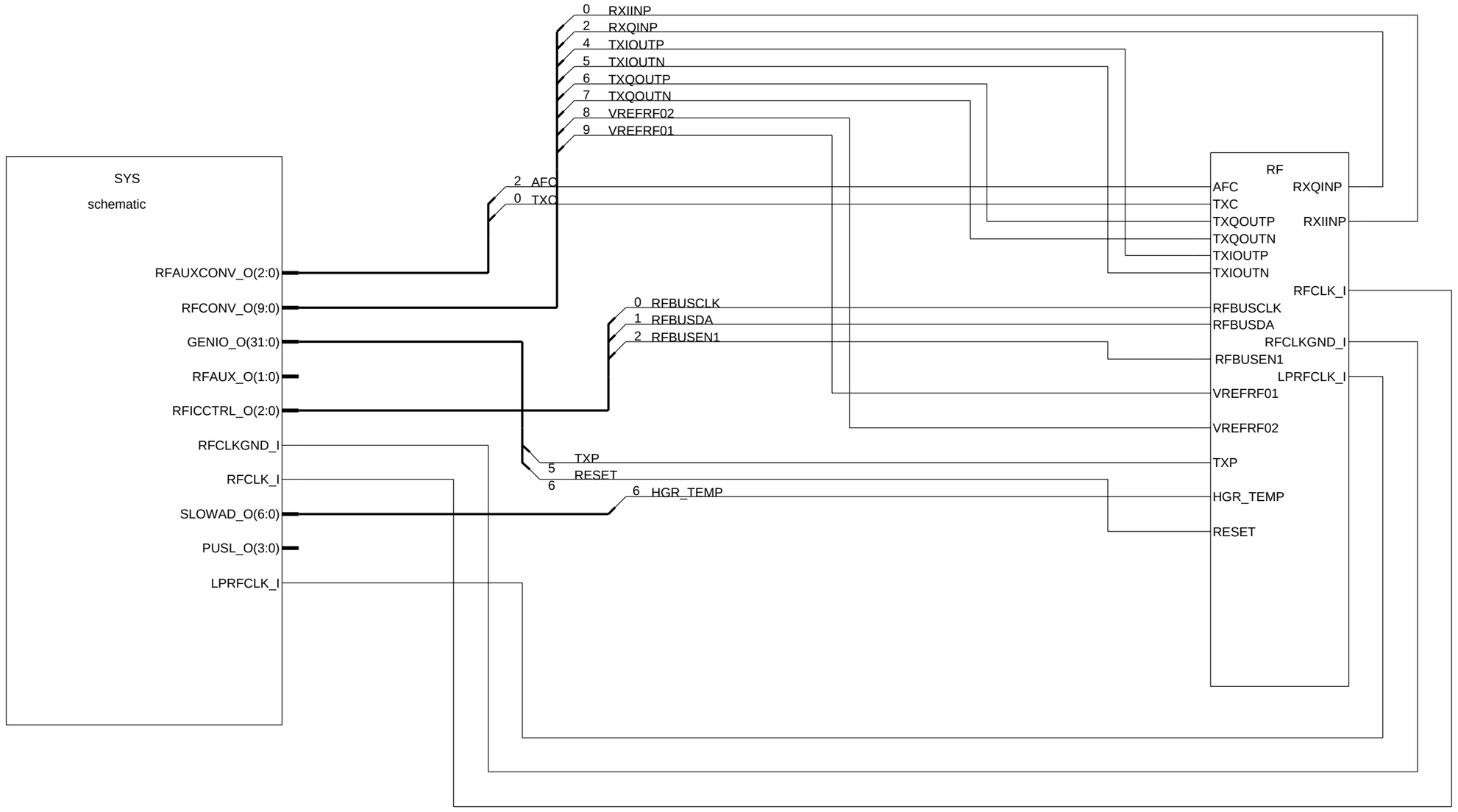
RF & BB Connection (Version 0.0 Edit 53) for layout version 20



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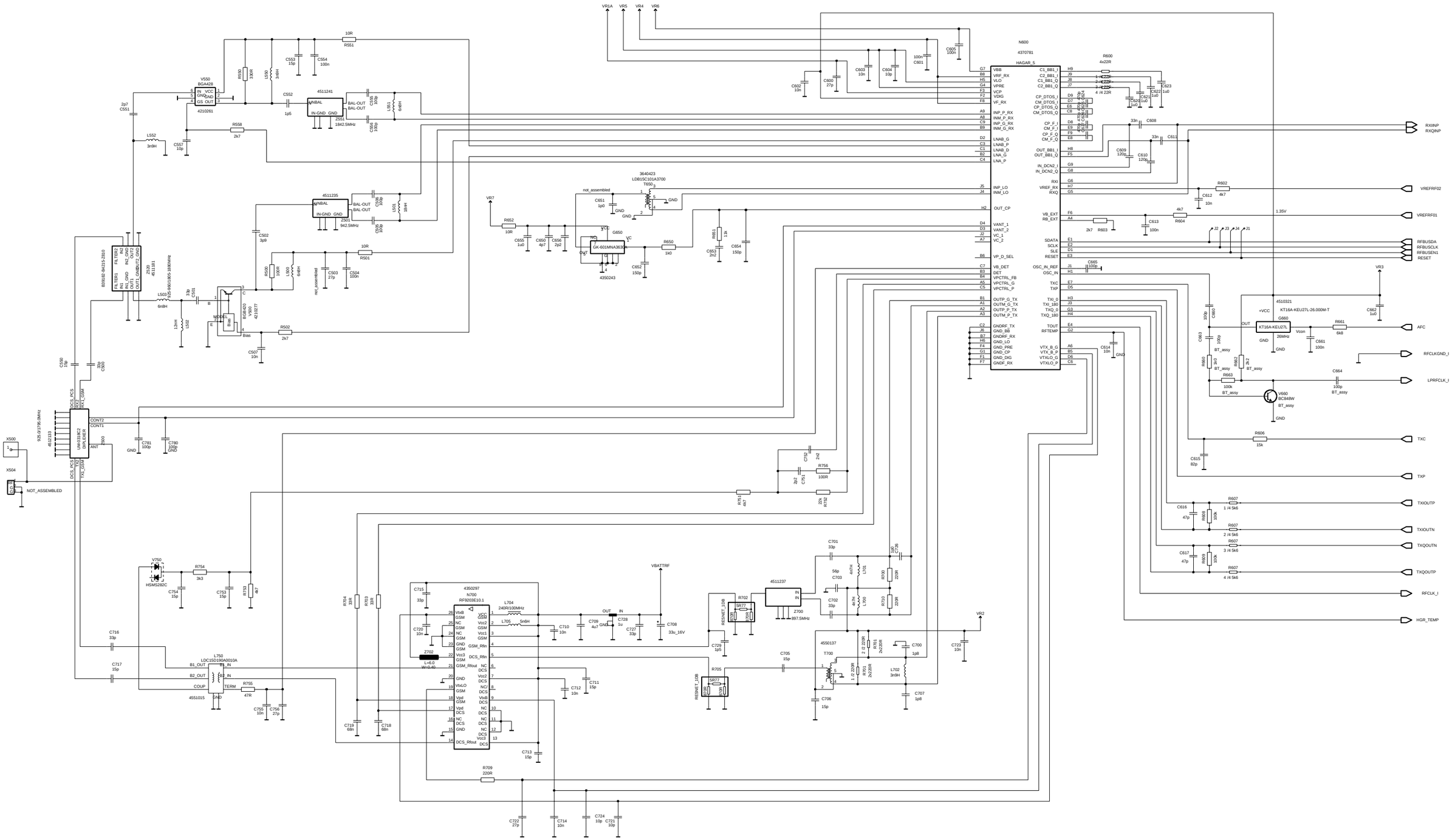
RF Schematic Diagram (Version 0 Edit 158) for layout version 20



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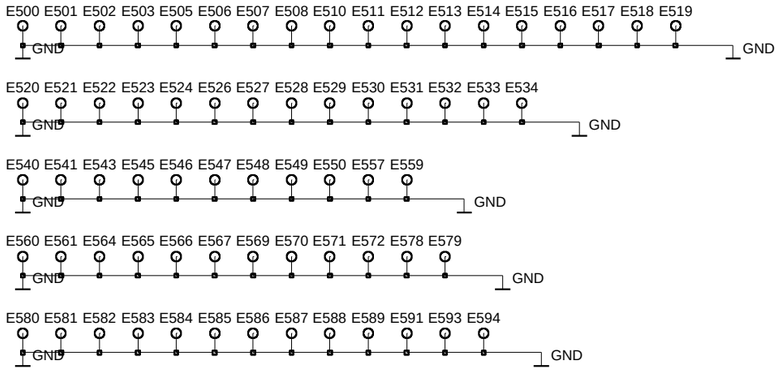
RF Gnd holes (Version 0 Edit 38) for layout version 20

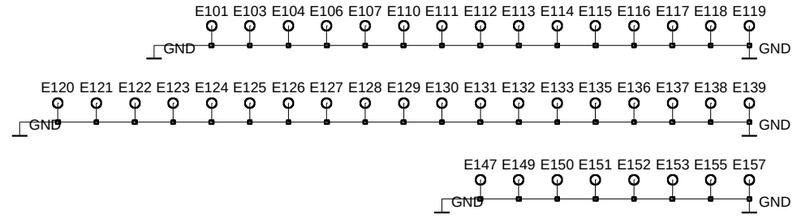
RF GLOBAL GND HOLES



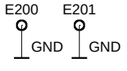
ADDED LIGHT GUIDE HOLES 1.3MM

PLACE 29.00 27.4

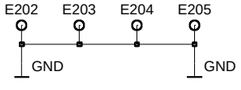
SYSTEM GLOBAL GND HOLES



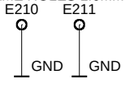
LIGHT GUIDE HOLES 1.3MM



SCREW HOLES 2.0MM

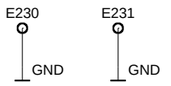


UI FRAME HOLES 1.6MM



DAMPER HOLE 2.0MM

GASGET HOLES 1.6MM AND 2.0MM



FRAME GUIDE HOLE 1.0MM

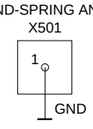
FRAME GUIDE HOLE 1.3MM

GASGET HOLES 1.4MM

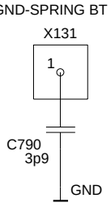
TOP GND-SPRING

SCREW HOLE TOP OF PHONE 2.0MM

GND-SPRING ANT



GND-SPRING BT



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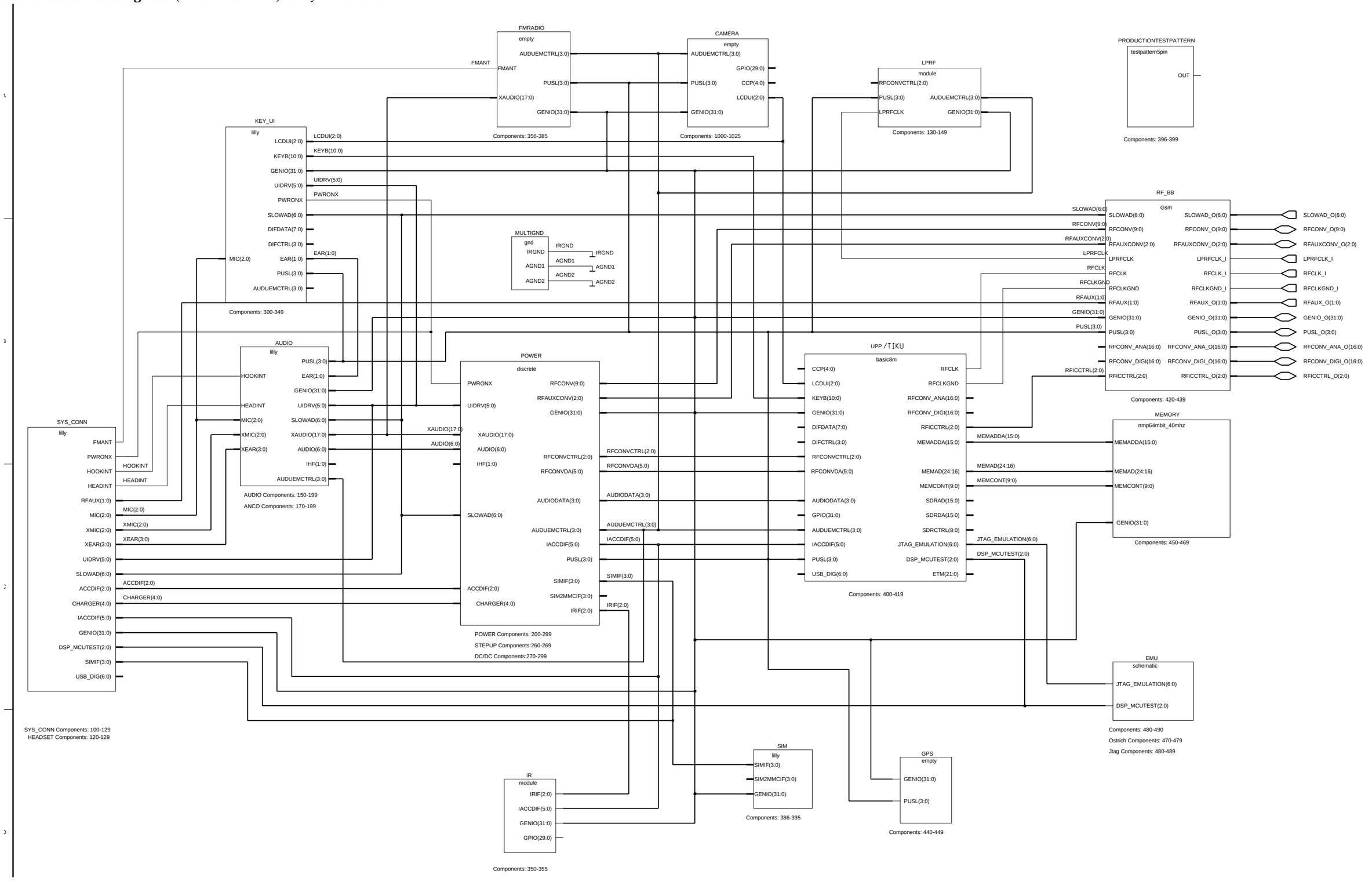
Baseband Block Diagram (Version 0 Edit 301) for layout version 20



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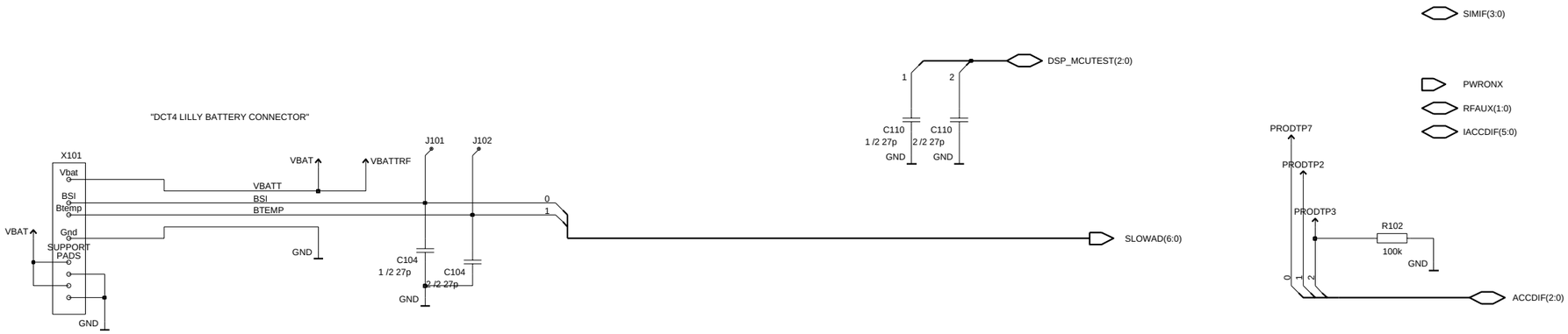
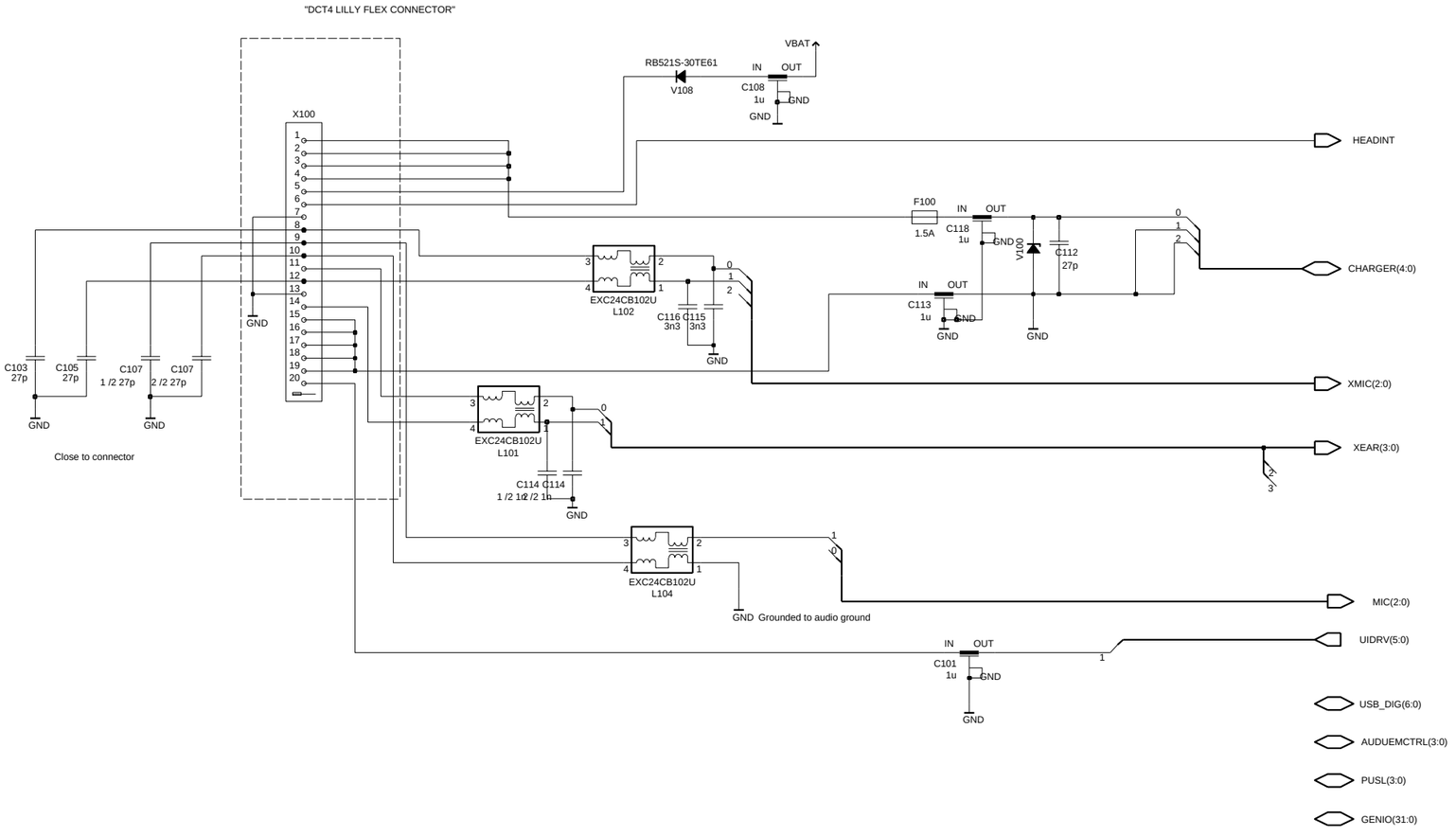
System Connector (Version 1.3 Edit 77) for layout version 20





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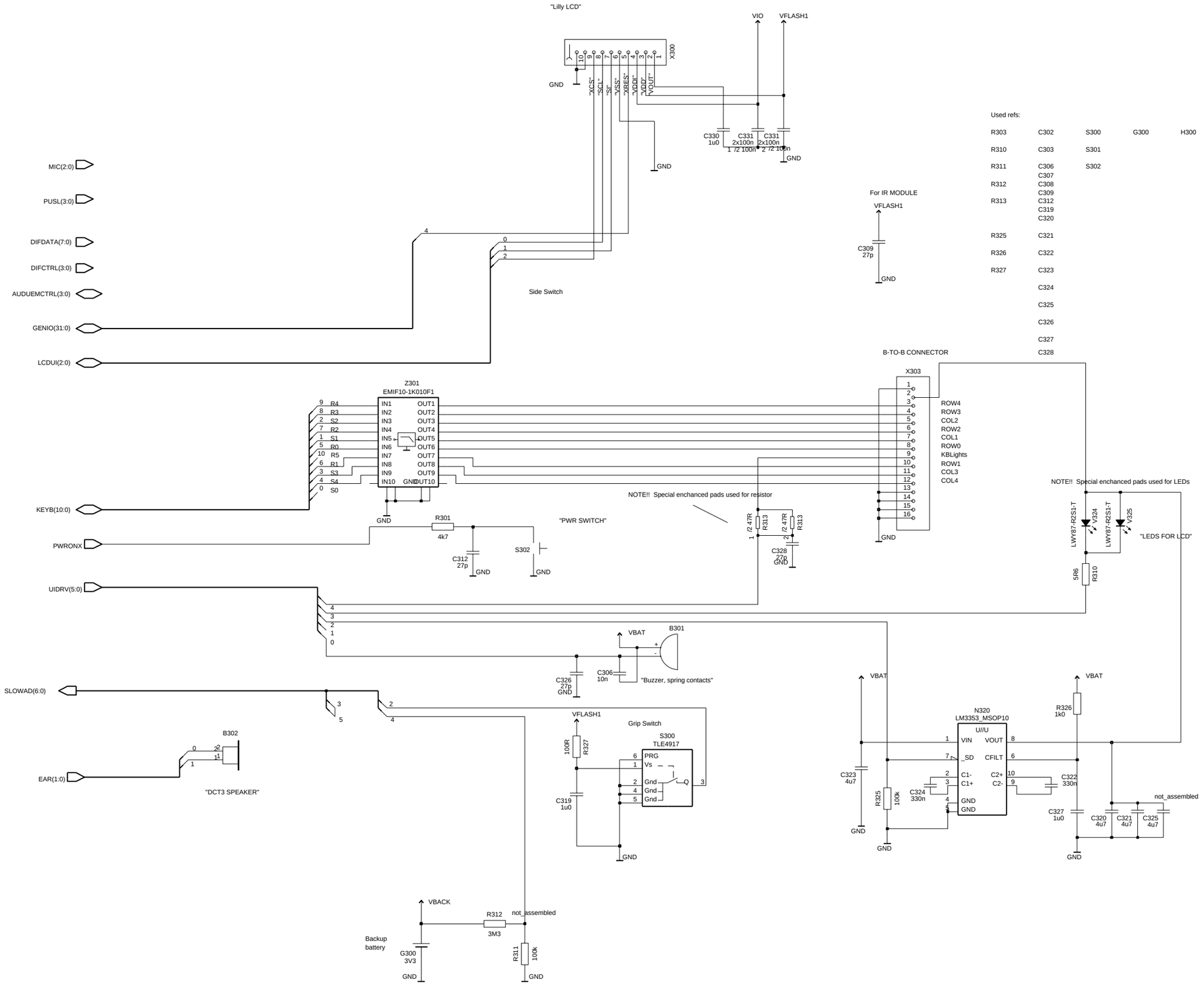
User Interface (Version 1.3 Edit 99) for layout version 20



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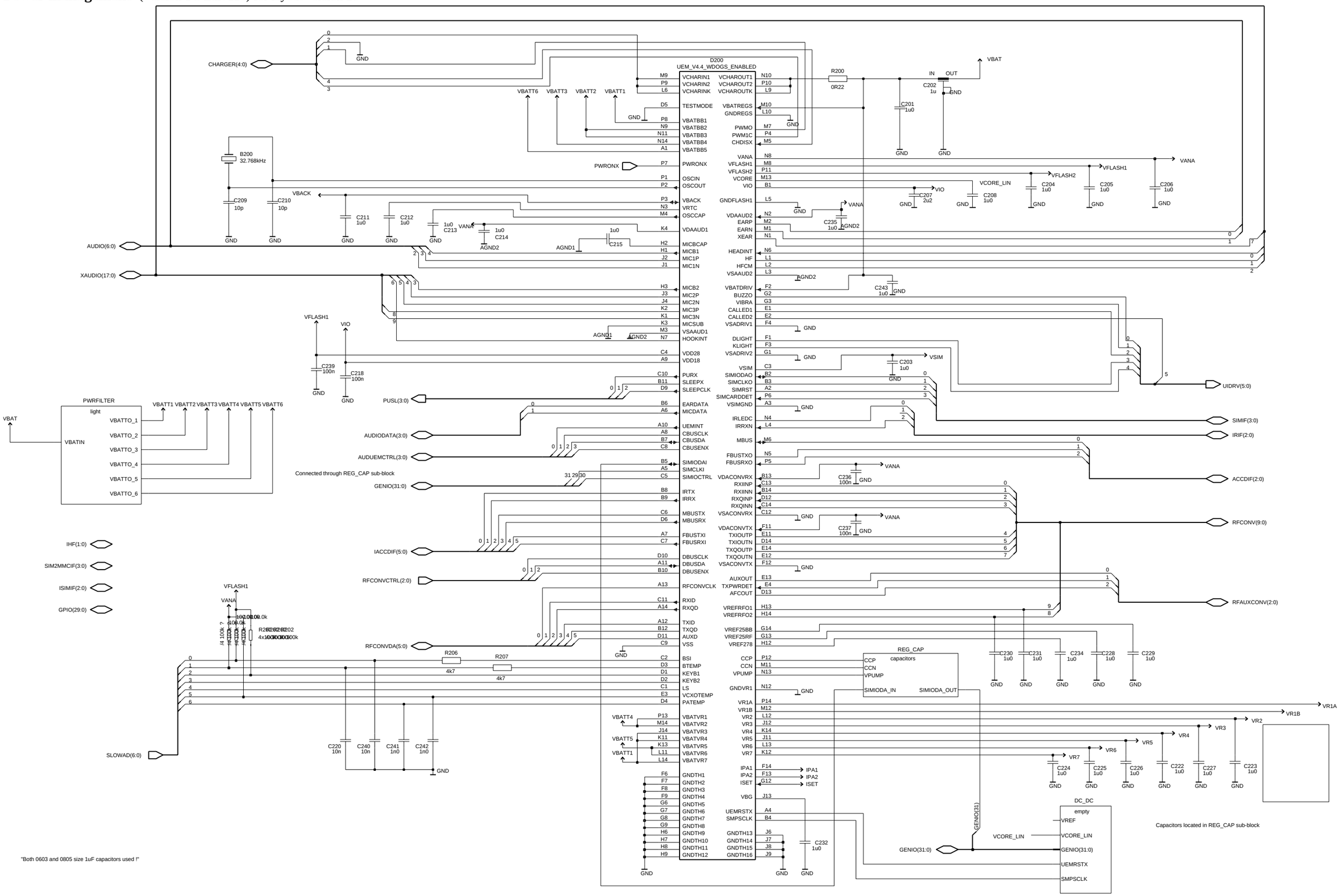
Power management (Version 1.3 Edit 110) for layout version 20



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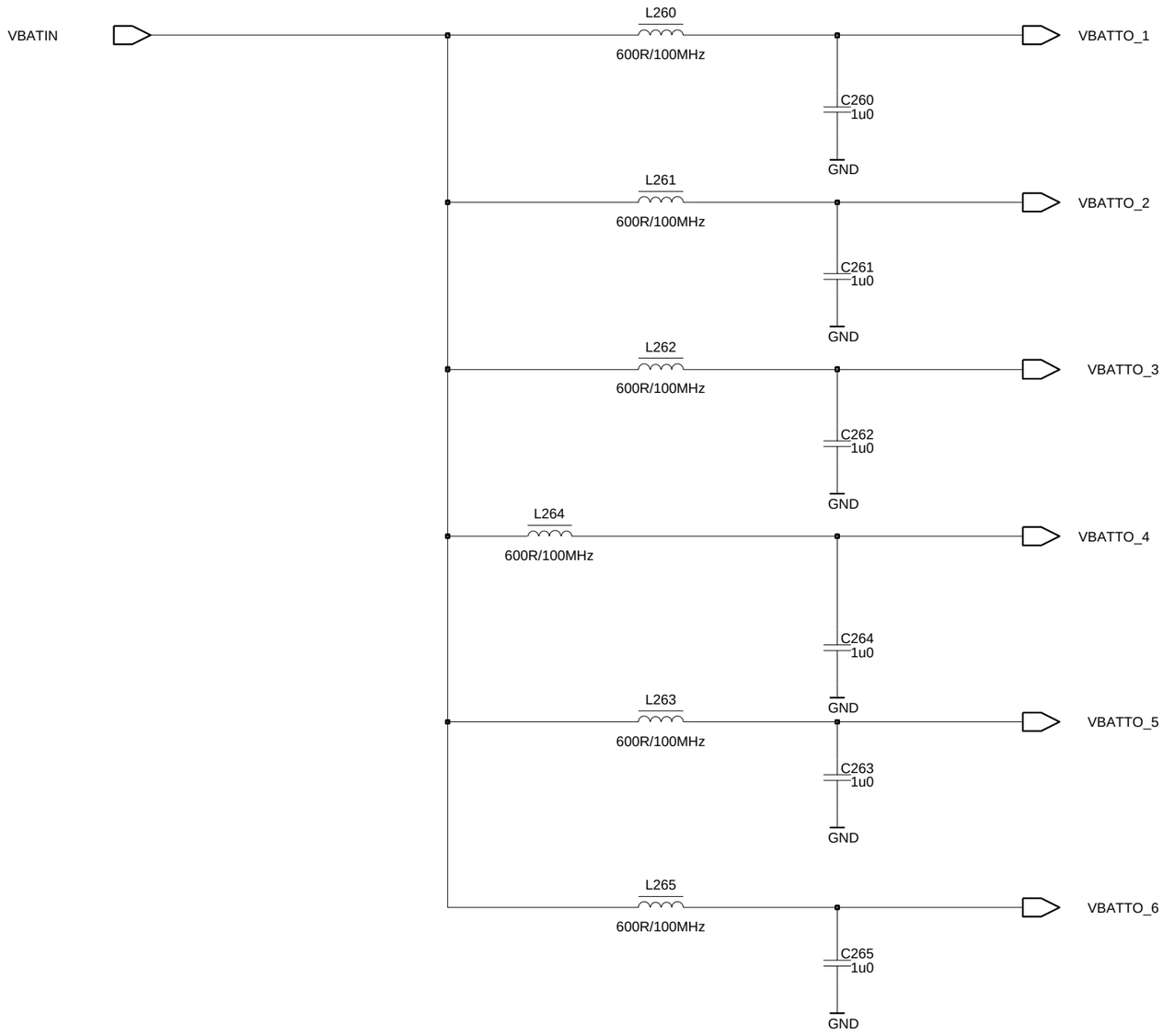
Light Filtering (Version 2.0 Edit 27) for layout version 20



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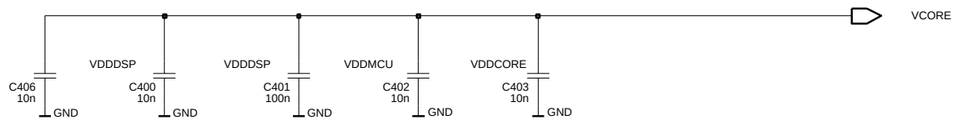
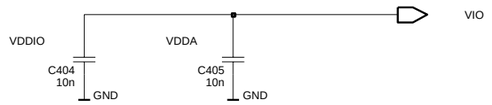
Discrete decoupling capacitors for UPP (v.1.3 ed. 10**)**





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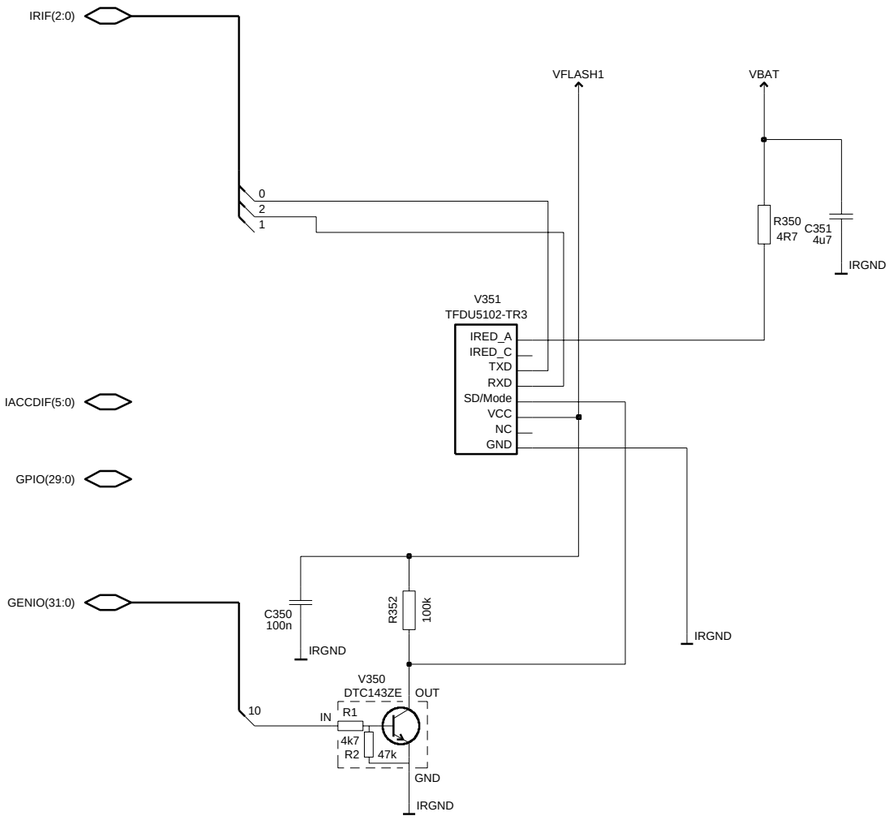
Infrared Module (Version 2.0 Edit 41) for layout version 20



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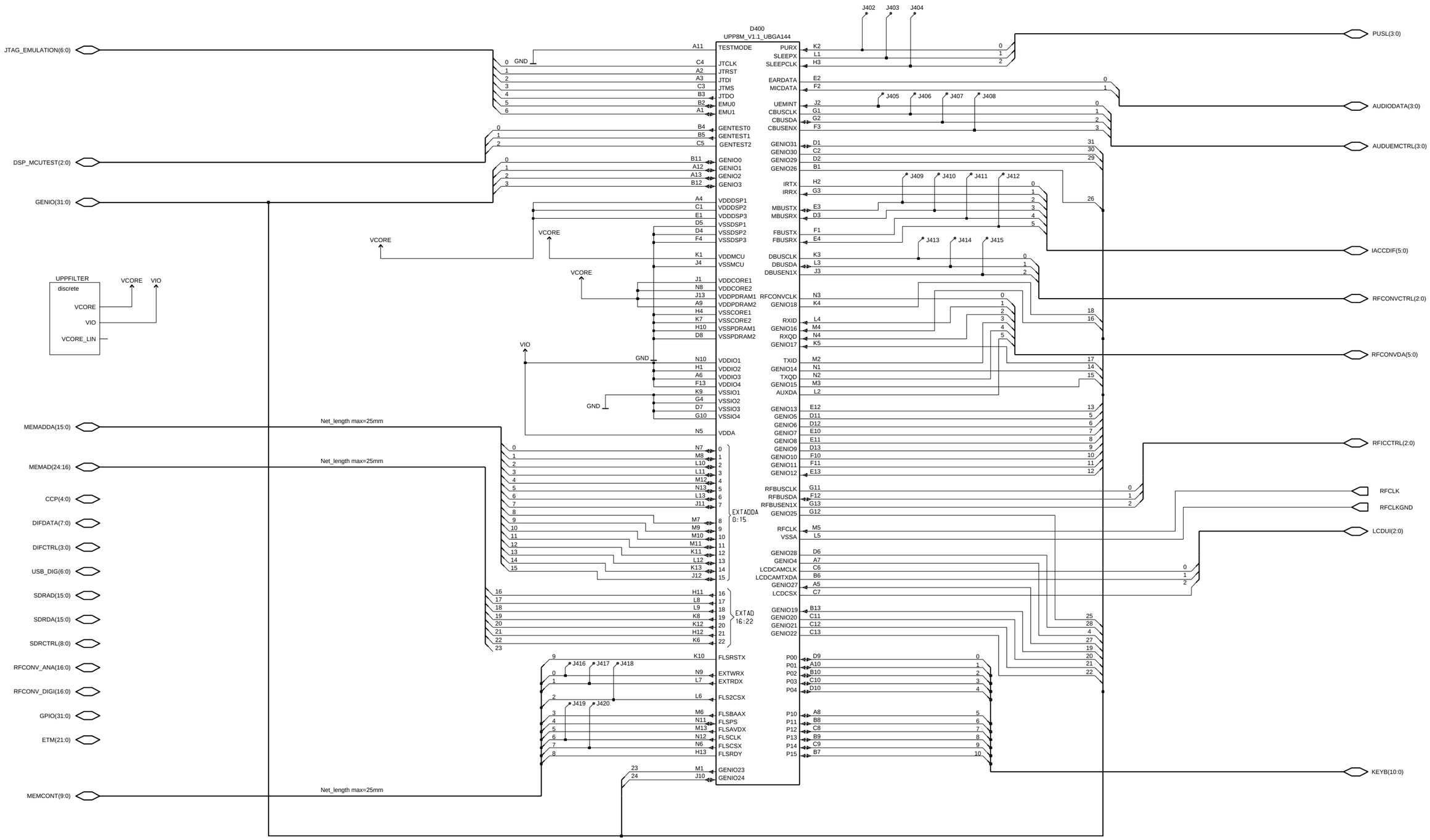

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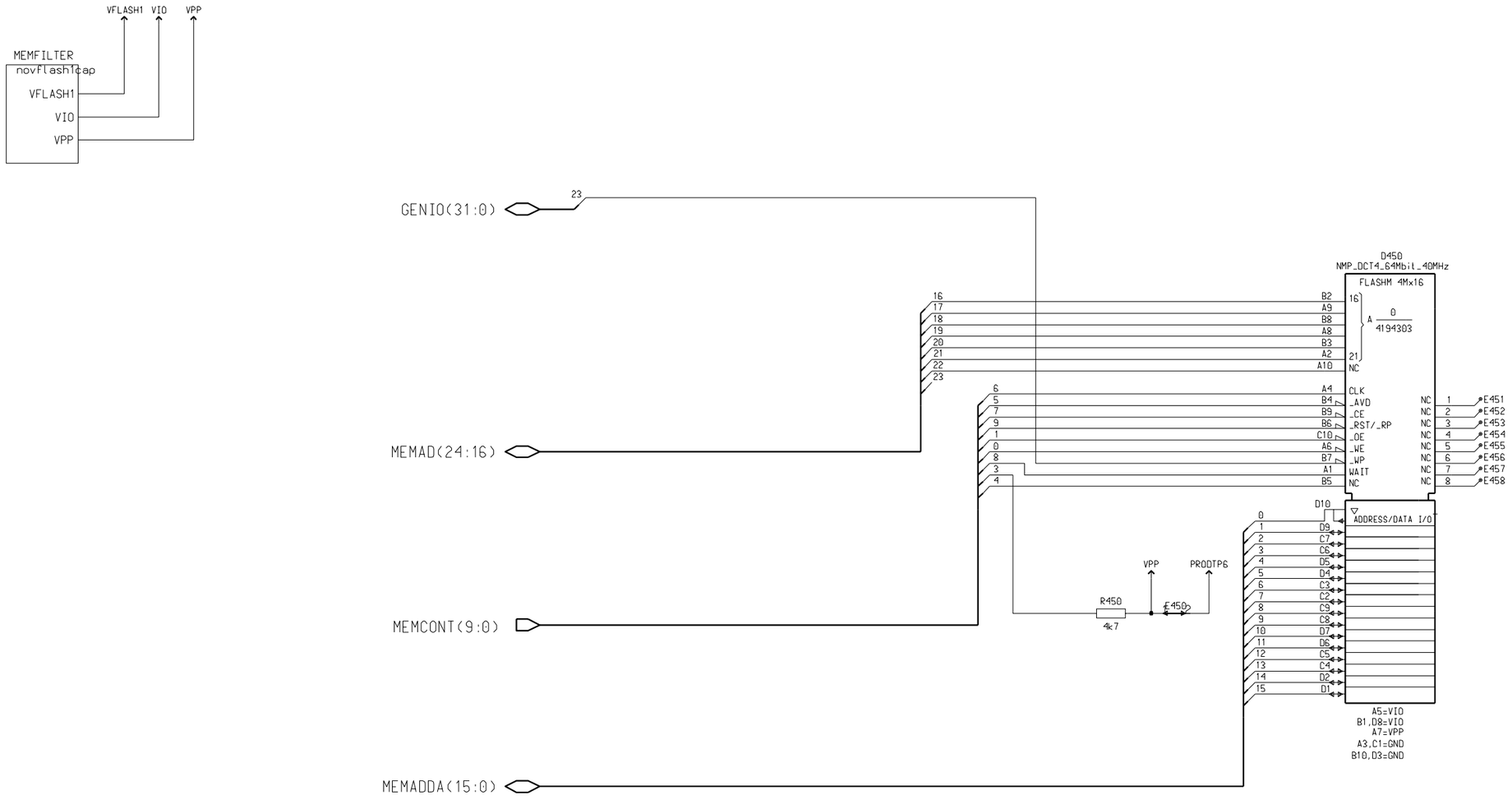
Flash Memory (Version 2.0 Edit 47) for layout version 20



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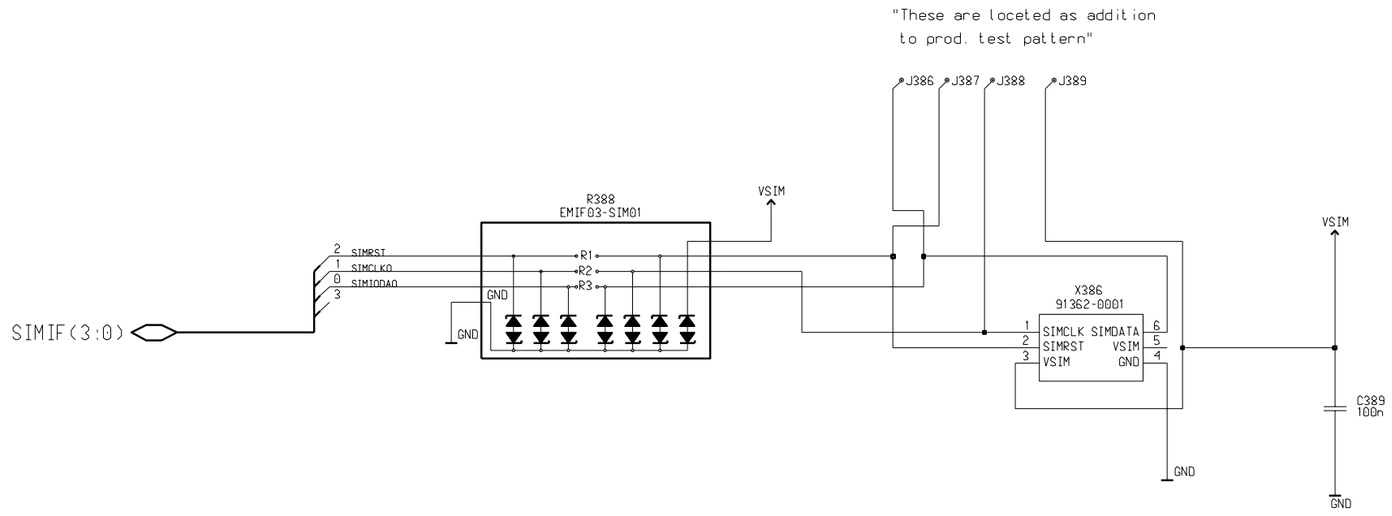
SIM Reader (Version 1.3 Edit 27) for layout version 20



GENIO(31:0)

SIM2MMCIF(3:0)

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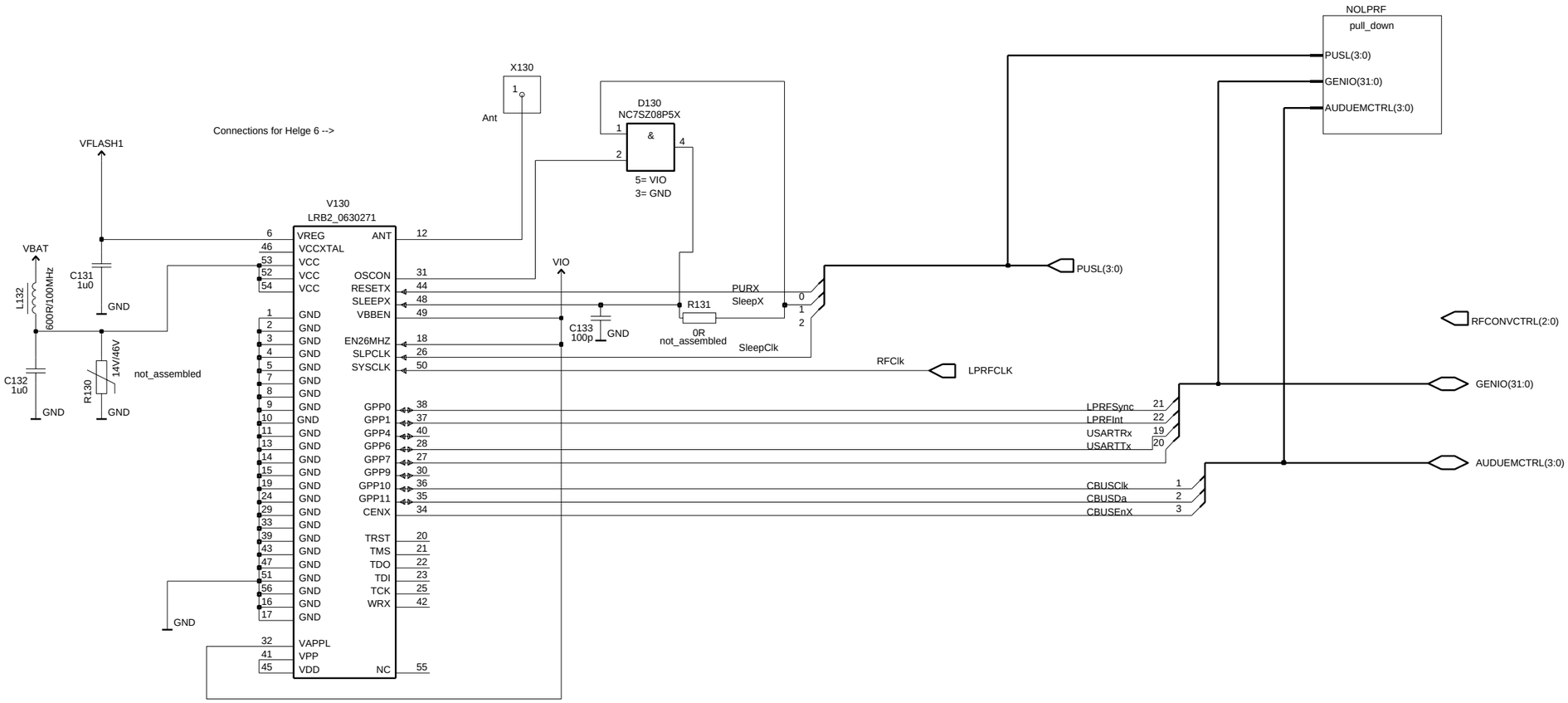
Bluetooth BT102 module (Version 1.3 Edit 69) for layout version 20



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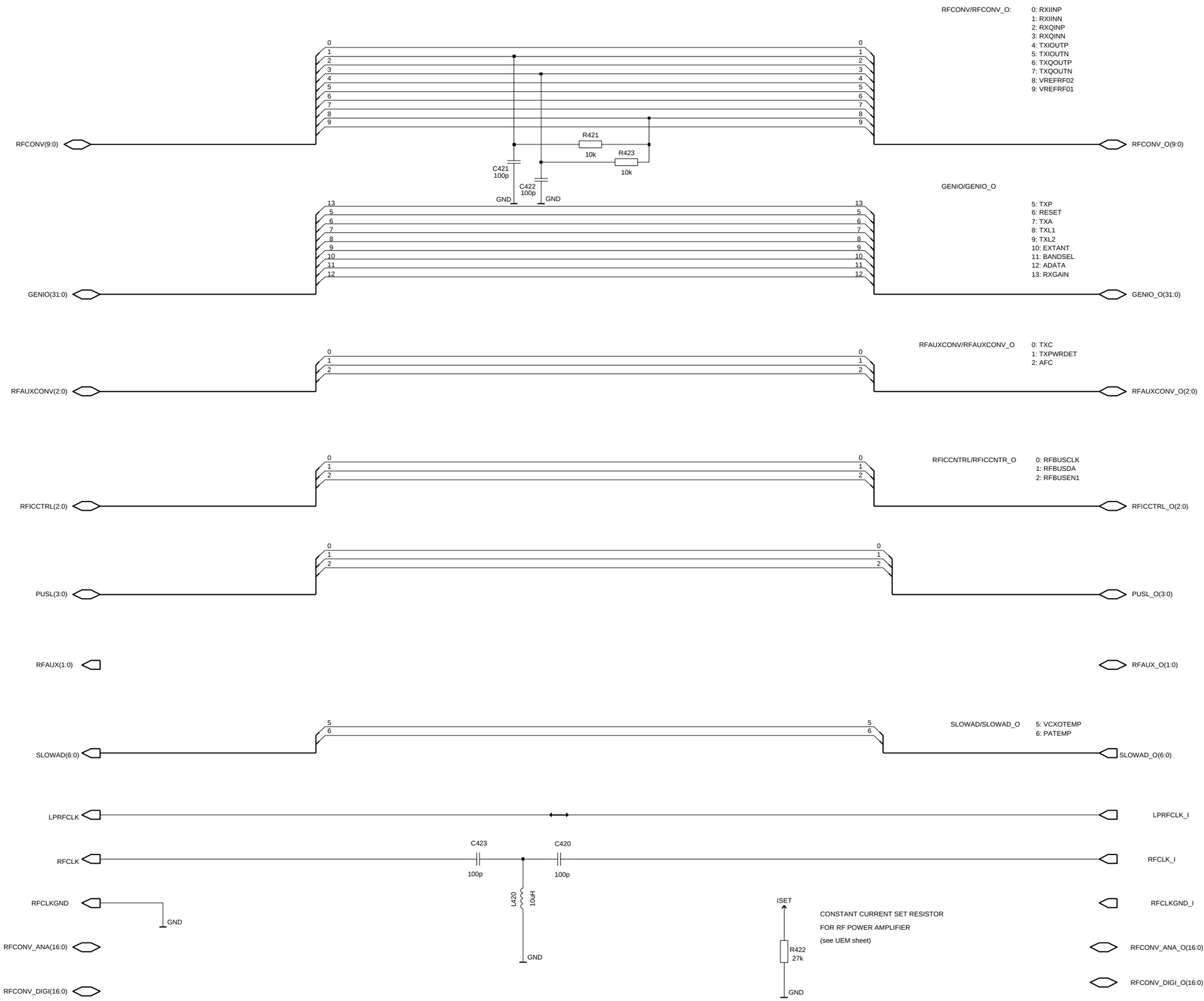
GSM RF - BB Interface (Version 1.3 Edit 41) for layout version 20



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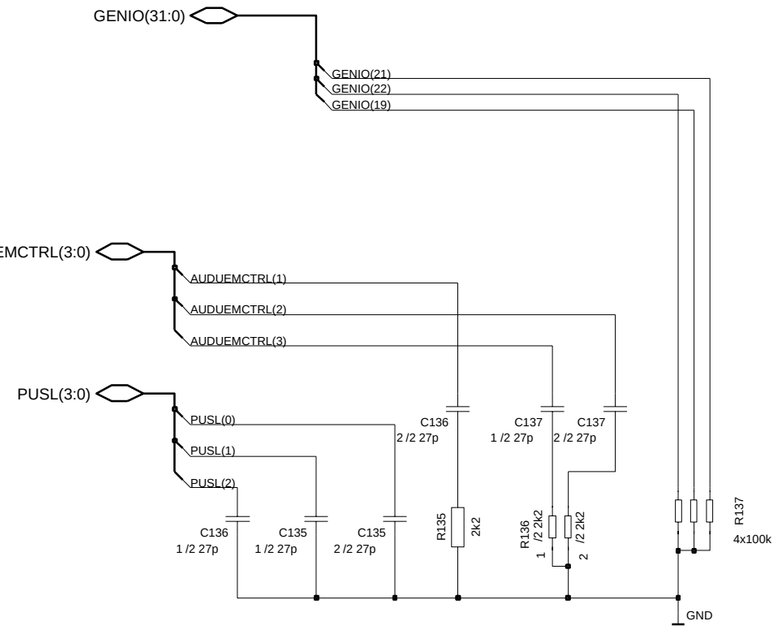
Pull down if no LPRF (Version 0 Edit 11) for layout version 20



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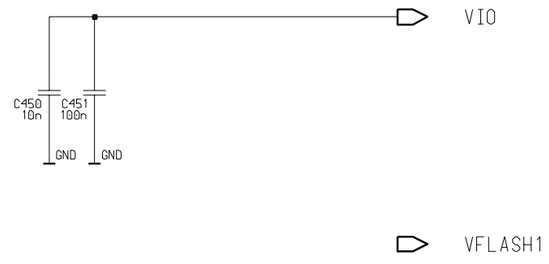
Discrete capacitors for memory without VFlash1 (Version 1.3 Edit 10) for layout version 20



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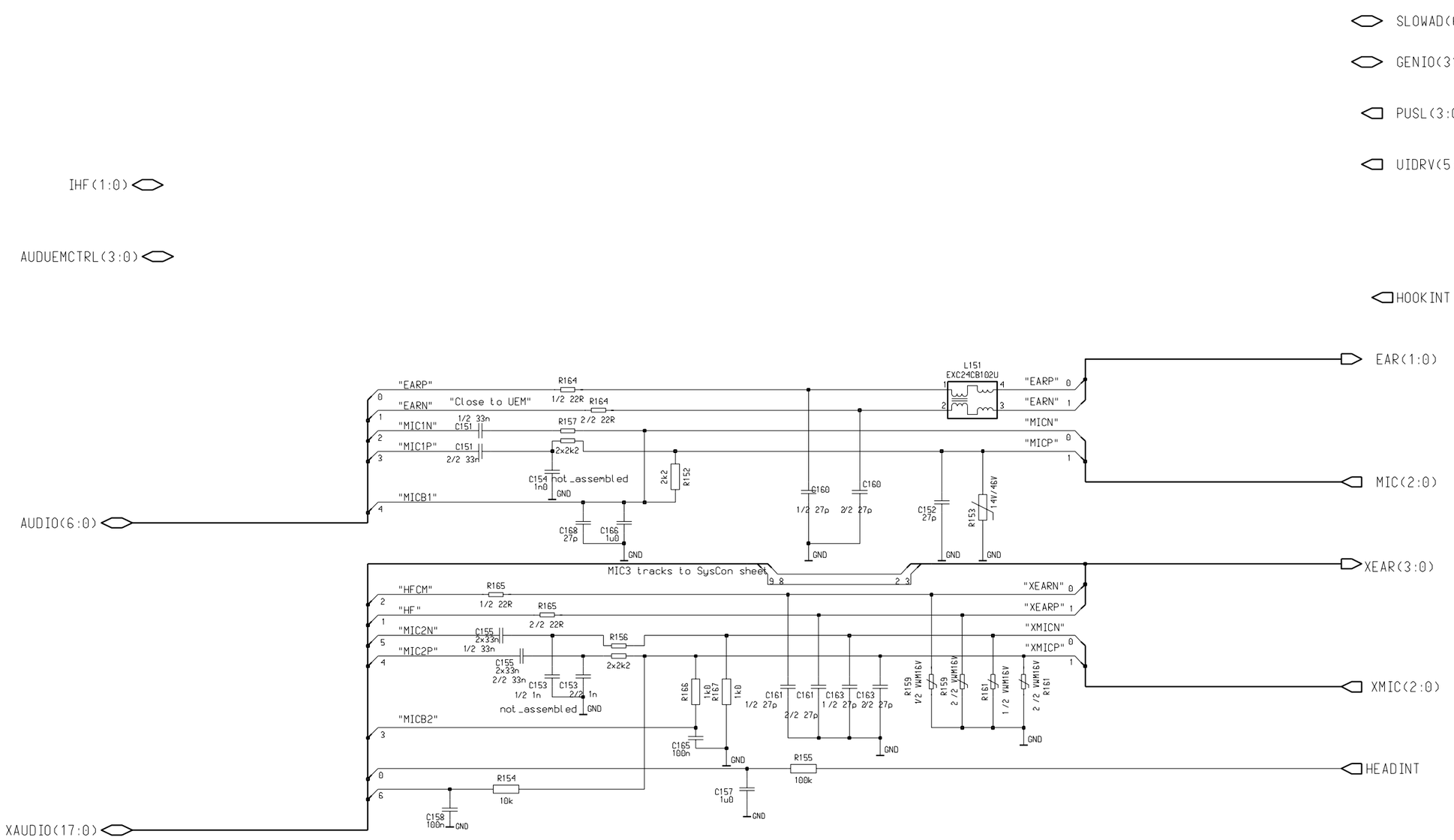

Used Refs: C151-C153, C155- 166
R151, 153-R160, 162, 163
L151

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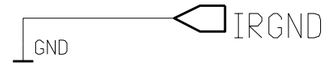
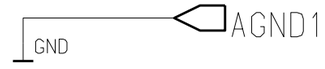
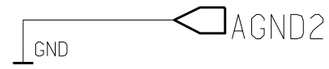
MultiGND symbol bypass (Version 0.0 Edit 8) for layout version 20







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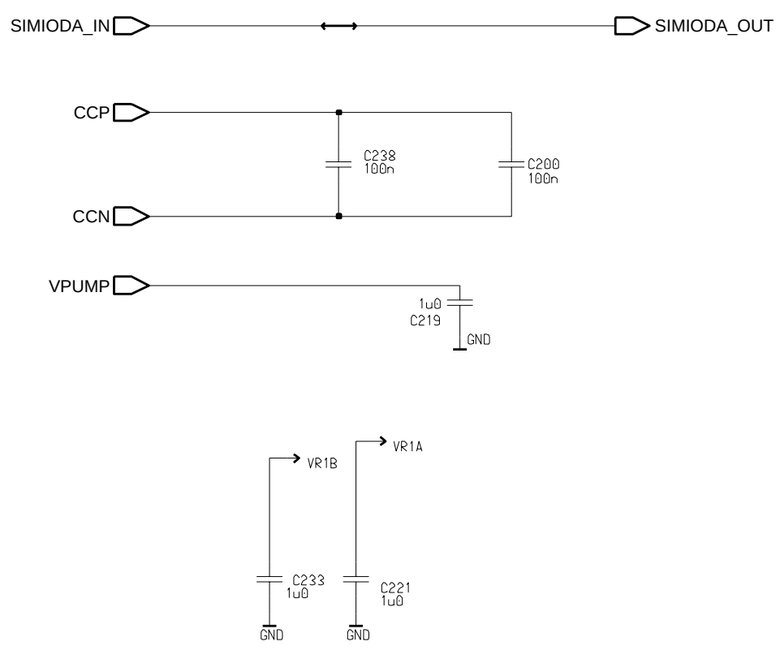
Old power discrete used (v.0 ed.6)



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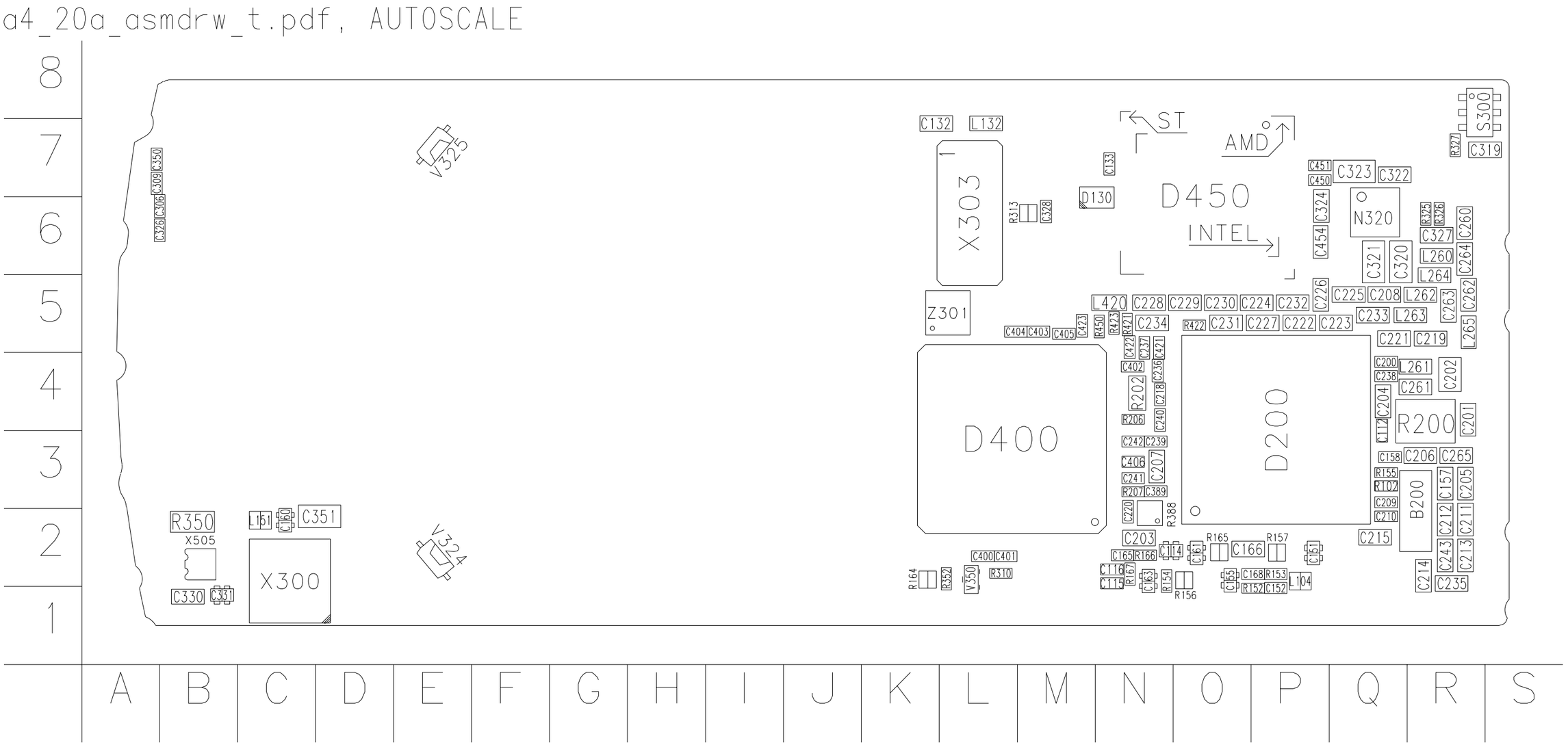
Component layout diagram, top, version 20



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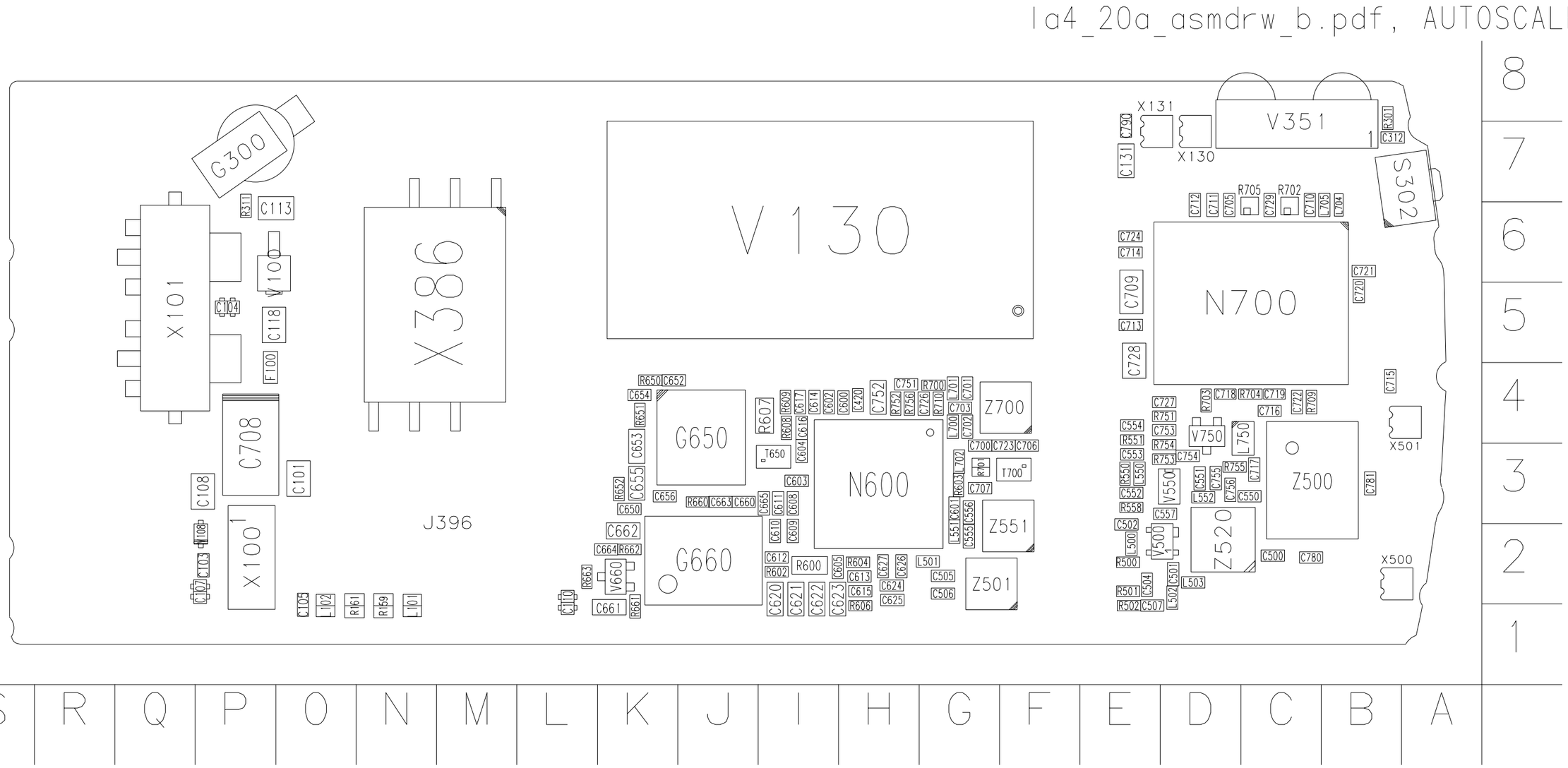
Component layout diagram, bottom, version 20



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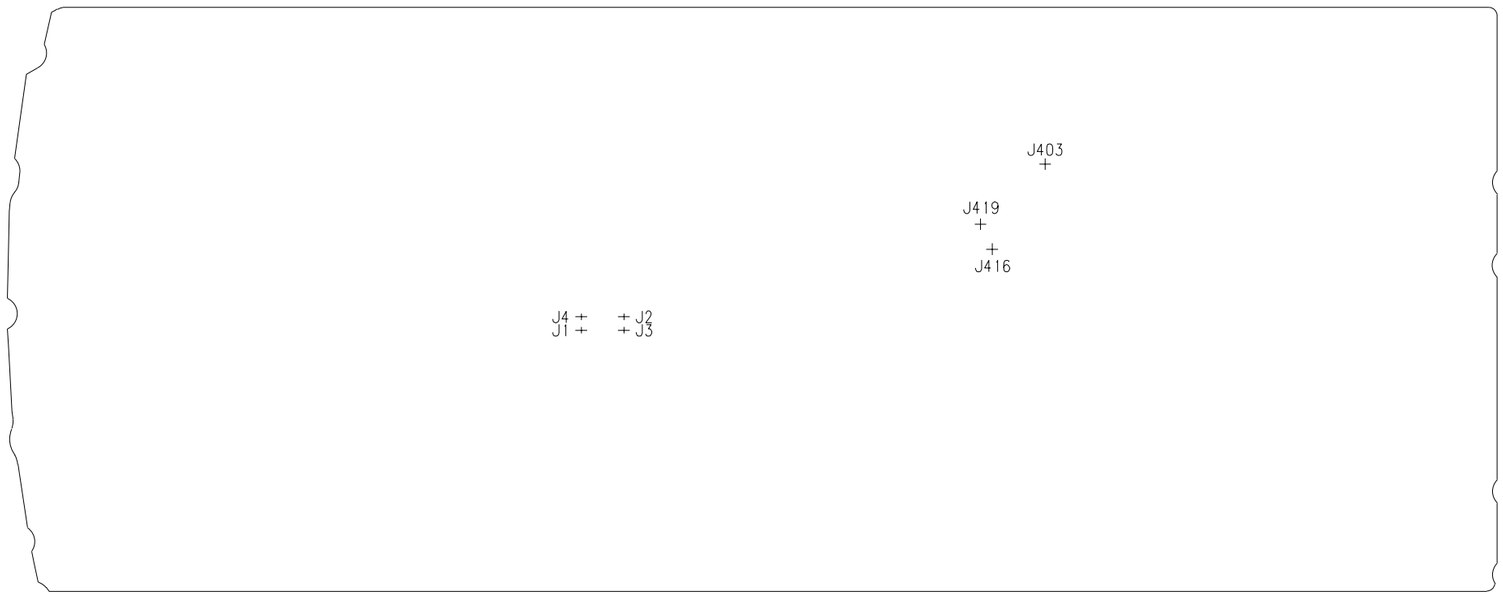
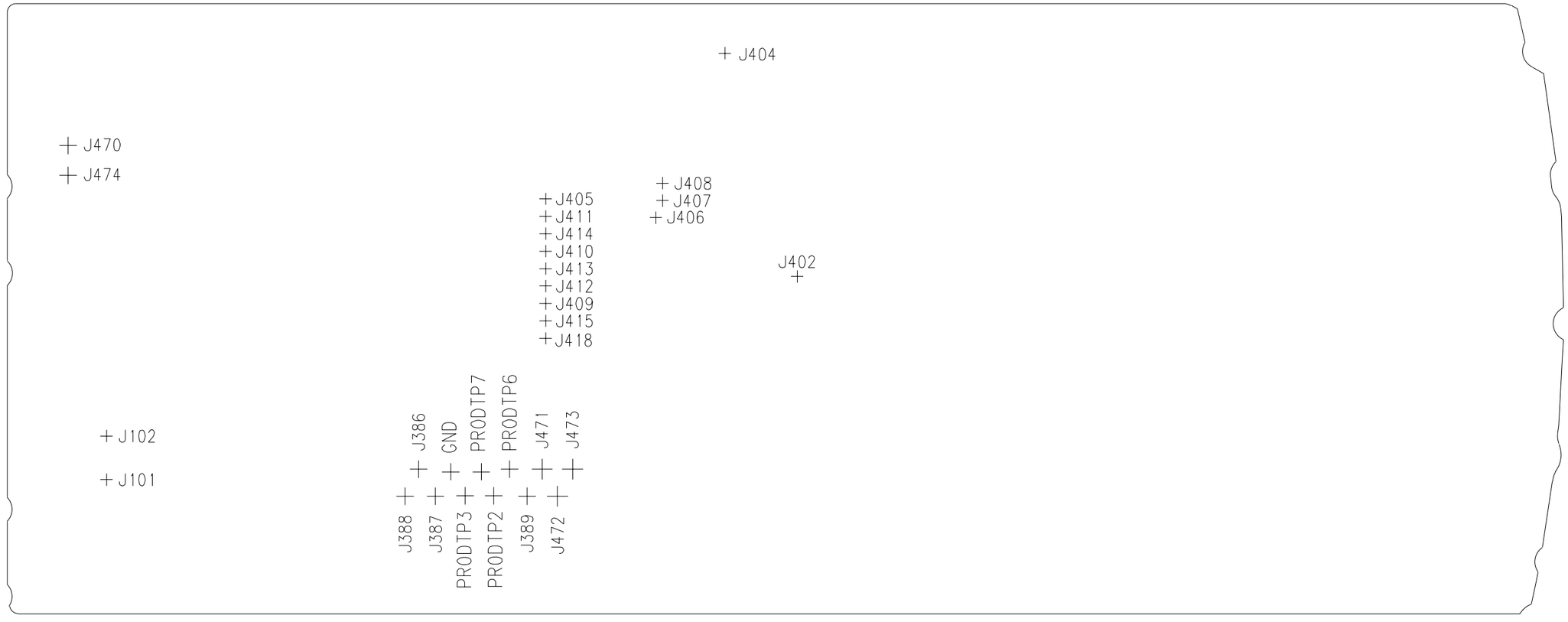
Test points pcb v_20, top



Test points pcb v_20, bottom



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